ART FILM - detail1

NOTES: UNLESS OTHERWISE SPECIFIED

1. SPECIFICATIONS/TOLERANCES:
   A. FABRICATE PER IPC-6012, CLASS 2, USING PROVIDED DATA FILES 600-60610-01_01.TGZ OR 610-60610-01_01.ZIP.
   B. ALL SPECIFICATIONS USED SHALL BE PER THEIR LATEST REVISIONS.
   C. THE DIMENSIONS OF CIRCUIT FEATURES IN THE PROVIDED DATA MAY BE ADJUSTED ONLY TO COMPENSATE FOR PROCESS TOLERANCES; ADDING, REMOVING OR RELOCATING CIRCUIT FEATURES, INCLUDING NON-FUNCTIONAL PADS, IS NOT ALLOWED, AND THE DESIGN OF ALL PLANE STRUCTURES MUST BE MAINTAINED TO ENSURE PROPER ELECTRICAL PERFORMANCE.
   D. REMOVE ALL BURRS AND BREAK SHARP EDGES, .381 [.015] MAX RADIUS.
   E. PARENTHETICAL INFORMATION IS FOR REFERENCE ONLY.
   F. REPAIR OF PCB DEFECTS IS NOT PERMITTED.

2. DIELECTRIC MATERIAL:
   A. DIELECTRIC MATERIAL SHALL BE PER 370HR MUST CONFORM TO UL94V-0 (RoHS COMPLIANT EPOXY-GLASS).
   B. MINIMUM DIELECTRIC THICKNESS SHALL BE .051 [.002] FOR REFERENCED STACK-UP DIMENSIONS OF.076 [.003] OR GREATER; IPC-6012 REQUIREMENTS SHALL OTHERWISE APPLY. SINGLE-PLY CONSTRUCTION IS ALLOWED.
   C. SEE LAYER STACK-UP FOR REQUIRED COPPER WEIGHTS AND THE FINISHED PCB THICKNESS. IF SPECIFIED, 1/3 OZ. STARTING FOIL MAY BE ACHIEVED BY 1/2 OZ. FOIL REDUCTION.
   D. FINISHED PCB THICKNESS SHALL BE MEASURED OVER LANDS AND/OR CONDUCTORS NOT COVERED BY SOLDER MASK.

3. DRILLING:
   A. VIA DIAMETERS (TOL. = +.051/- DRILL DIAMETER [+.0020/- DRILL DIAMETER]) SHALL BE VERIFIED BEFORE PLATING; ALL OTHER HOLE DIAMETERS SHALL BE VERIFIED AT FINAL INSPECTION.
   B. LAYER-TO-LAYER MISREGISTRATION SHALL BE .127 [.005] MAXIMUM.

4. SOLDER MASK:
   A. APPLY LPI SOLDER MASK USING PROVIDED DATA.
   B. SOLDER MASK SHALL BE PER IPC-SM-840, CLASS T, COLOR BLUE.
   C. THE DIMENSIONS OF SOLDER MASK-DEFINED PADS ON PLANES AND/OR WIDE CONDUCTORS SHALL NOT BE MODIFIED.

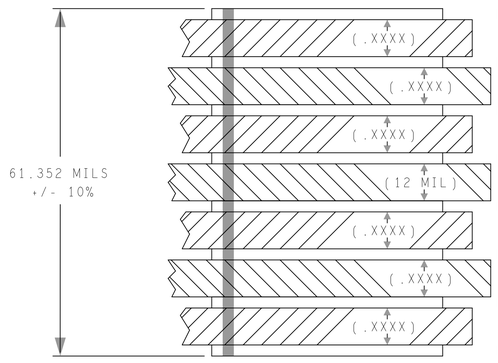
5. MARKING:
   A. MARK PCB PER PROVIDED DATA USING SILKSCREEN OR AUTOMATED INJET PROCESSING WITH PERMANENT, NON-CONDUCTIVE INK, COLOR WHITE.
   B. SUPPLIER ID AND TRACEABILITY INFORMATION SHALL BE APPLIED USING PERMANENT, NON-CONDUCTIVE INK, COLOR WHITE.
   C. INK SHALL NOT BE APPLIED TO ANY SOLDERABLE SURFACE.

6. ELECTRICAL TEST:
   A. DESIGN VERIFICATION SHALL BE DONE PRIOR TO PCB FABRICATION USING SUPPLIED VALOR ODB++ DATABASE, OR GERBER DATA AND AN IPC-D-356 NETLIST.
   B. ALL PCBS SHALL BE 100% ELECTRICALLY TESTED FOR OPENS AND SHORTS USING PROVIDED DATA.
   C. APPLY TEST STAMP IN NON-LEGEND AREA ON REAR SIDE OF PCB; OK TO APPLY TO PANEL RAILS IF SPACE DOES NOT PERMIT.

7. FINAL FINISH:
   A. FINAL FINISH SHALL BE ELECTROLESS NICKEL/IMMERSION GOLD (ENIG) PER IPC-4552.

8. IMPEDANCE:
   A. IMPEDANCE TOLERANCE SHALL BE +/- 10%.
   B. SEE LAYER STACK-UP FOR IMPEDANCE REQUIREMENTS.

9. IF PANELIZATION SPECIFICATIONS ARE PROVIDED, THE PCBS SHALL BE DELIVERED IN PANEL FORM. HOWEVER, THESE SPECIFICATIONS MAY BE CHANGED AS REQUIRED BY THE CONTRACT MANUFACTURER TO SUPPORT VOLUME ASSEMBLY REQUIREMENTS.



LAYER DESCRIPTION	FINISHED COPPER WT	SE IMP OHMS	SE TRACE WIDTH	REF LAYER	CPW SPACE	DIFF IMP OHMS	DIFF TRACE WIDTH/SPACE	REF LAYER	CPW SPACE
L01 - TOP	1.0 OZ	50E	7.2 MILS	02	------	90E 100E	6/6 MILS 5/7 MILS	02	------
L02 - PLANE	1.0 OZ	--	-----	---	------	---	----	---	------
L03 - SIGNAL	1.0 OZ	50E	5 MILS	02	------	---	,-----/,-----	---	------
L04 - PLANE	1.0 OZ	--	,-----	---	------	---	,-----/,-----	---	------
L05 - PLANE	1.0 OZ	--	,-----	---	------	---	,-----/,-----	---	------
L06 - SIGNAL	1.0 OZ	50E	5 MILS	07	------	90E	5/6.7 MILS	07	------
L07 - PLANE	1.0 OZ	--	-----	---	------	---	----	---	------
L08 - BOTTOM	1.0 OZ	50E	7.2 MILS	07	------	90E 100E	6/6 MILS 5/7 MILS	07	------

STACK-UP

SEE BOM	SEE BOM
NEXT ASSY	USED ON
APPLICATION	

THE INFORMATION CONTAINED HEREIN IS CONFIDENTIAL AND PROPRIETARY TO CYPRESS SEMICONDUCTOR AND SHALL NOT BE REPRODUCED OR DISCLOSED IN WHOLE OR IN PART OR USED FOR ANY DESIGN, MANUFACTURE, OR OTHERWISE, EXCEPT WHEN SUCH USER POSSESSES AUTHORIZATION FROM CYPRESS

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN METRIC WITH INCHES IN BRACKETS
.XXX +.064 [+.005] .XX +.13 [+.01] ANGLES +.5°

MATERIAL 2

FINISH 7

DO NOT SCALE DRAWING

APPROVALS	DATE
DRAWN HUSA	14/11/22
ENGINEER MISHRASANATK	14/11/22
CHECKER	
QA -	-
PROJ. ENG. -	-

198 CHAMPION COURT
SAN JOSE, CA 95134
(408) 943-2600

TITLE: PCB FABRICATION, DEMO FX3_U3V CAMOI Base Board

SIZE	CAGE CODE	CY P/N
D	-	610-60625-01

SCALE	SHEET	REV
1/1	1 OF 2	01

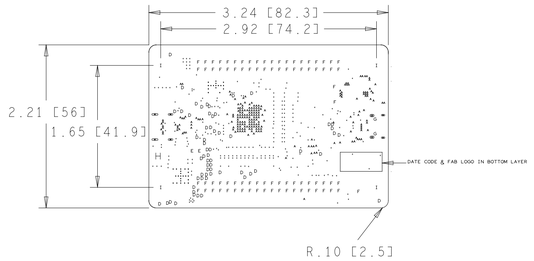
COMPUTER GENERATED DRAWING
DO NOT CHANGE MANUALLY

ALLEGRO FILE: 600-60610-01_CYUSB3KIT-004 EZ-USB SX3 EXPLORER BASE BOARD LAYOUT_REV01.BRD

FAB NOTES REV 04/05/17

ART FILM - detail1

DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN MILS				
FIGURE	FINISHED_SIZE	TOLERANCE_DRILL	PLATED	QTY
A	8.0	+3.0/-3.0	PLATED	218
B	9.84	+3.0/-3.0	PLATED	38
C	10.0	+3.0/-3.0	PLATED	254
D	12.0	+3.0/-3.0	PLATED	61
E	39.37	+3.0/-3.0	PLATED	2
F	40.16	+3.0/-3.0	PLATED	83
G	31.5	+2.0/-2.0	NON-PLATED	2
H	86.61	+2.0/-2.0	NON-PLATED	2
I	118.0	+2.0/-2.0	NON-PLATED	4
PROVIDE PAD IN PASTE	47.244x21.654	+3.0/-3.0	PLATED	2
PROVIDE PAD IN PASTE	55.118x33.465	+3.0/-3.0	PLATED	2
PROVIDE PAD IN PASTE	62.992x23.622	+0.0/-0.0	PLATED	2
PROVIDE PAD IN PASTE	82.677x23.622	+0.0/-0.0	PLATED	2
			TOTAL HOLES:	672



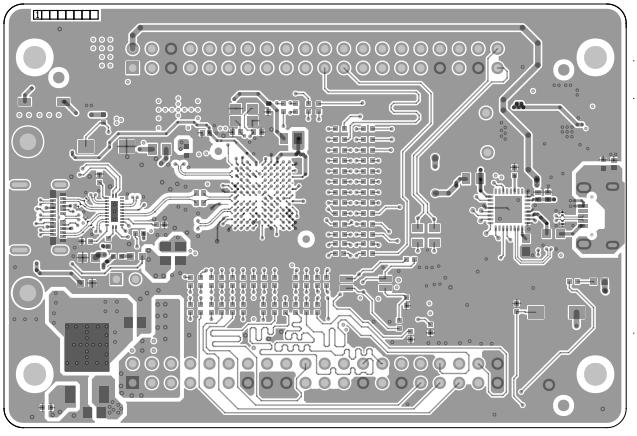
THE INFORMATION CONTAINED HEREIN IS CONFIDENTIAL AND PROPRIETARY TO CYPRESS SEMICONDUCTOR AND SHALL NOT BE REPRODUCED OR DISCLOSED IN WHOLE OR IN PART OR USED FOR ANY DESIGN, MANUFACTURE, OR OTHERWISE, EXCEPT WHEN SUCH USER POSSESSES DIRECT, WRITTEN AUTHORIZATION.

SIZE	CAGE CODE	CY P/N
D	-	610-60625-01
SCALE		SHEET / REV
1/1		2 OF 2 / 01

COMPUTER GENERATED DRAWING
DO NOT CHANGE MANUALLY

ALLEGRO FILE: 600-60610-01_CYUSB3KIT-004 EZ-USB SX3 EXPLORER BASE BOARD LAYOUT_REV01.BRD

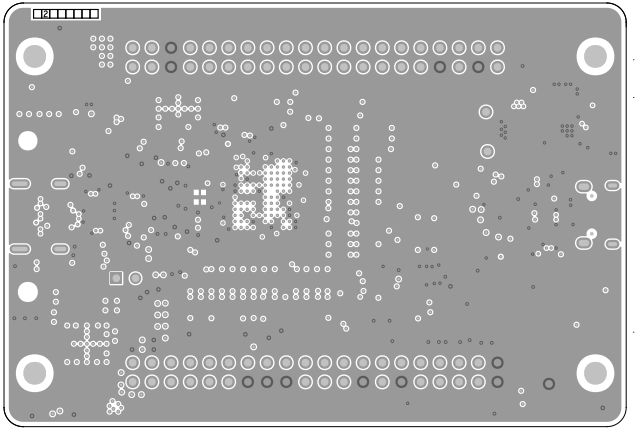
ART FILM - TOP



SAN JOSE, CA 95134 (408) 943-2600	PROJECT: DEMO_FX3_U3V_CAM01 Base Board		
	DRAWN BY: HUSA		
	LAYER: TOP SIDE		
	DWG NO: 600-60625-01	REV: 01	DATE: 14/11/22

ART FILM - TOP

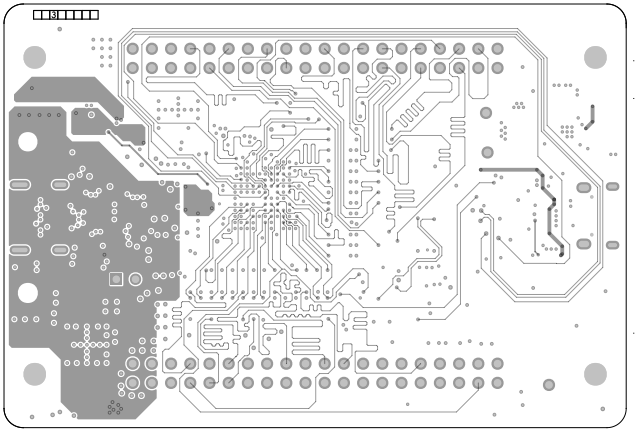
ART FILM - L02_GND1



Infineon SAN JOSE, CA 95134 (408) 943-2600	PROJECT: DEMO_FX3_U3V_CAM01 Base Board		
	DRAWN BY: HUSA		
	LAYER: 02_GND1		
	DWG NO: 600-60625-01	REV: 01	DATE: 14/11/22

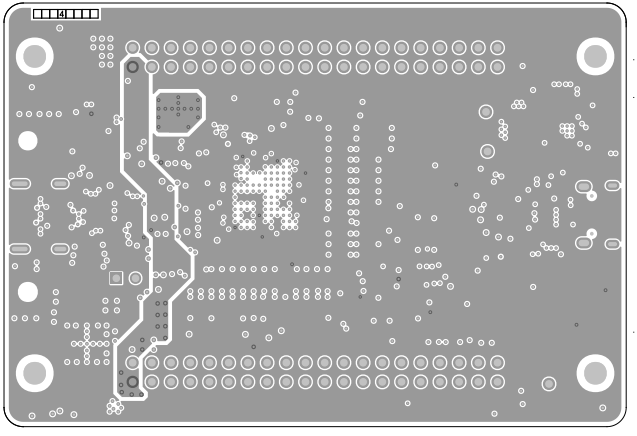
ART FILM - L02_GND1

ART FILM - L03_SIG1



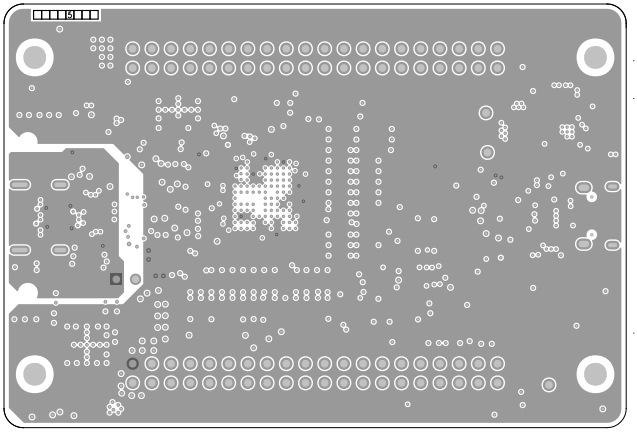
Infineon SAN JOSE, CA 95134 (408) 943-2600	PROJECT: DEMO_FX3_U3V_CAM01 Base Board		
	DRAWN BY: HUSA		
	LAYER: 03_SIG1		
	DWG NO: 600-60625-01	REV: 01	DATE: 14/11/22

ART FILM - L03_SIG1



Infineon SAN JOSE, CA 95134 (408) 943-2600	PROJECT: DEMO_FX3_U3V_CAM01 Base Board		
	DRAWN BY: HUSA		
	LAYER: 04_PWR1		
	DWG NO: 600-60625-01	REV: 01	DATE: 14/11/22

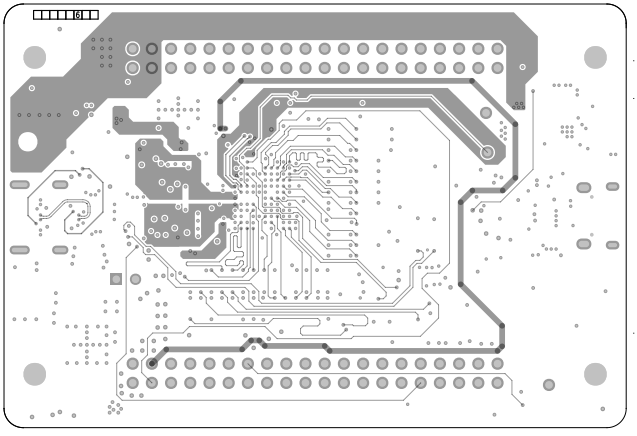
ART FILM - L05_PWR2



Infineon SAN JOSE, CA 95134 (408) 943-2600	PROJECT: DEMO_FX3_U3V_CAM01 Base Board		
	DRAWN BY: HUSA		
	LAYER: 05_PWR2		
	DWG NO: 600-60625-01	REV: 01	DATE: 14/11/22

ART FILM - L05_PWR2

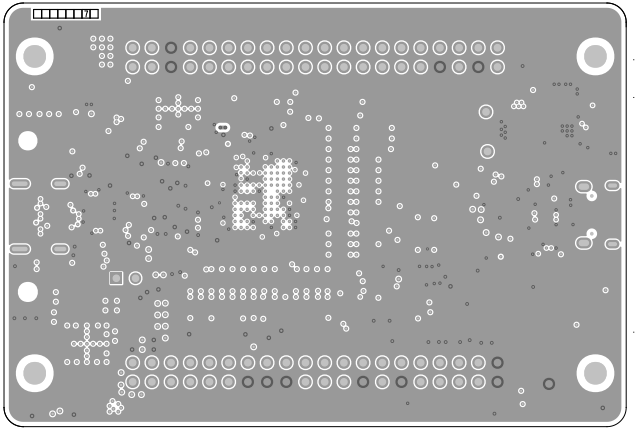
ART FILM - L06_SIG2



Infineon SAN JOSE, CA 95134 (408) 943-2600	PROJECT: DEMO_FX3_U3V_CAM01 Base Board		
	DRAWN BY: HUSA		
	LAYER: 06_SIG2		
	DWG NO: 600-60625-01	REV: 01	DATE: 14/11/22

ART FILM - L06_SIG2

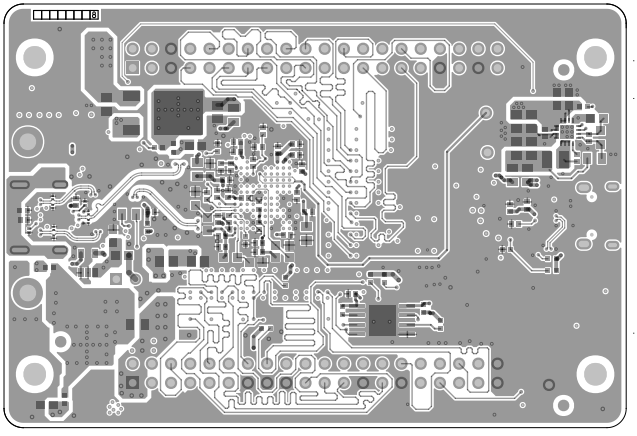
ART FILM - L07_GND2



Infineon SAN JOSE, CA 95134 (408) 943-2600	PROJECT: DEMO_FX3_U3V_CAM01 Base Board		
	DRAWN BY: HUSA		
	LAYER: 07_GND2		
	DWG NO: 600-60625-01	REV: 01	DATE: 14/11/22

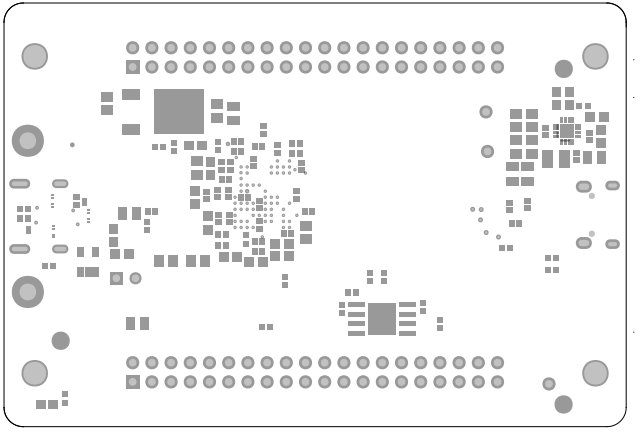
ART FILM - L07_GND2

ART FILM - BOTTOM

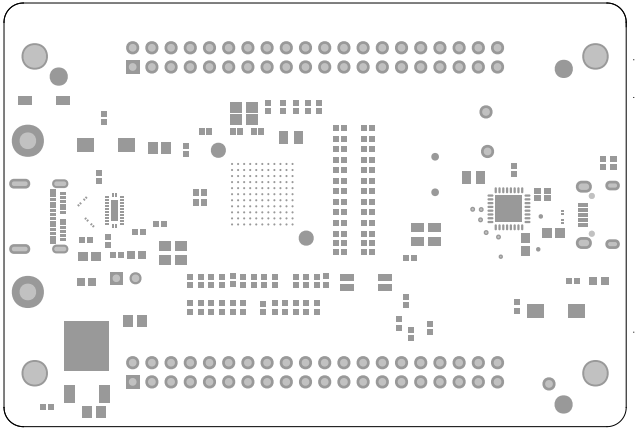


SAN JOSE, CA 95134 (408) 943-2600	PROJECT: DEMO_FX3_U3V_CAM01 Base Board		
	DRAWN BY: HUSA		
	LAYER: BOTTOM SIDE		
	DWG NO: 600-60625-01	REV: 01	DATE: 14/11/22

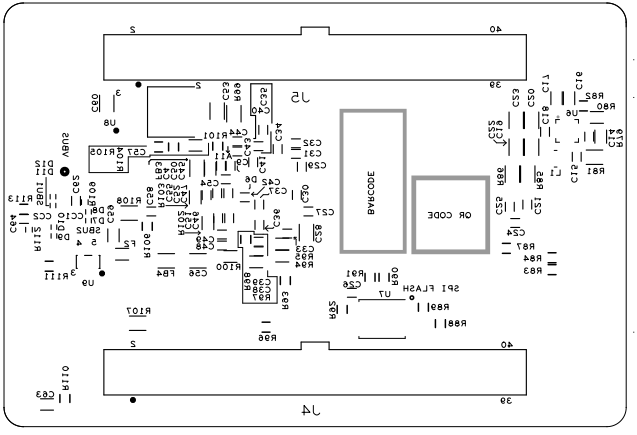
ART FILM - BOTTOM



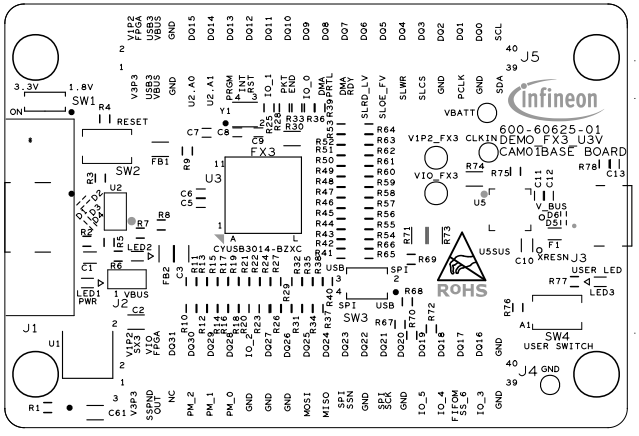
Infineon SAN JOSE, CA 95134 (408) 943-2600	PROJECT: DEMO_FX3_U3V_CAM01 Base Board		
	DRAWN BY: HUSA		
	LAYER: SOLDERMASK BOTTOM		
	DWG NO: 600-60625-01	REV: 01	DATE: 14/11/22



Infineon SAN JOSE, CA 95134 (408) 943-2600	PROJECT: DEMO_FX3_U3V_CAM01 Base Board		
	DRAWN BY: HUSA		
	LAYER: SOLDERMASK TOP		
	DWG NO: 600-60625-01	REV: 01	DATE: 14/11/22



Infineon SAN JOSE, CA 95134 (408) 943-2600	PROJECT: DEMO_FX3_U3V_CAM01 Base Board		
	DRAWN BY: HUSA		
	LAYER: SILKSCREEN BOTTOM		
	DWG NO: 600-60625-01	REV: 01	DATE: 14/11/22



Infineon SAN JOSE, CA 95134 (408) 943-2600	PROJECT: DEMO_FX3_U3V_CAM01 Base Board		
	DRAWN BY: HUSA		
	LAYER: SILKSCREEN TOP		
	DWG NO: 600-60625-01	REV: 01	DATE: 14/11/22